REMARKS

In an office action dated September 3 2003, the Examiner rejected claims 1-6 and 17-21 under 35 U.S.C. §102(e) as anticipated by Bosshart (US Patent 6,049,231). Claims 7-16 were allowed.

The claims are unamended. Applicants respectfully traverse the rejections of the claims.

As explained in the background section of the specification herein, applicant's invention is directed to reducing or eliminating the so-called parasitic bi-polar transistor effect in silicon-on-insulator integrated circuits. Unlike conventional integrated circuits using bulk silicon as a substrate, silicon-on-insulator circuits pose certain special design challenges. Among these is the fact that, because the gate is not grounded to the substrate, it can float to a high potential if the potentials at both the source and drain are simultaneously high. This phenomenon can cause a small current leakage through the gate even when it should be shut off, an effect referred to as a parasitic bi-polar transistor effect. If the transistor in question is coupled to a pre-charge node of a dynamic logic circuit, the pre-charge can be drained to an intermediate node even if the transistor is gated off, which could cause erroneous logic signals to be propagated. In accordance with applicants' preferred embodiment, this tendency is corrected by discharging the intermediate node, preferably by using a gated discharge path to ground, the gate for the discharge path using the same input as the gate between the pre-charge node and the intermediate node.

It should be emphasized that the problem addressed by applicants' invention does not occur in conventional integrated circuits using bulk silicon as the substrate, since the gate is inherently held at ground.

Bosshart, cited by the Examiner, discloses a dynamic logic circuit having pre-charge nodes and intermediate nodes, but does not disclose the particular problem addressed by applicants' invention. *Bosshart* is rather directed to a technique for reducing the number of signal inversions in a dynamic multiplexer circuit, using certain logical manipulations. *Bosshart* does not disclose the type of substrate used in the construction of his integrated circuit, and it appears that the circuit is intended for use in conventional bulk silicon substrate construction.

Referring to claim 1, in the Office Action, the Examiner appears to read the recited "discharging device" on *Bosshart*'s feature 26_{DT}, which is the clocked discharge transistor, used to enable the logic (feature 26_L) to selectively discharge the pre-charge node during the evaluation phase of the clock cycle. Even if all other limitations of claim 1 are ignored, it should be clear that this reading is erroneous, because applicants' recited "discharging device" requires control from an input signal other than the clock, whereas *Bosshart*'s discharge transistor is controlled by the clock.

Claim 1 recites:

> 1. A method of eliminating parasitic bipolar transistor action in a Silicon on Insulator (SOI) Metal Oxide Semiconductor (MOS) device located in a logic circuit, said logic circuit being adapted to receive *an input signal and a clock signal*, the method comprising:
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> controlling the conduction of an active discharging device *with the input signal*, said active discharging device being coupled to an intermediate node of said logic circuit, whereby the parasitic bipolar transistor is deactivated. [emphasis added]

Claim 1 plainly recites a separate "input signal" and "clock signal", and further recites that the active discharging device is controlled "with the input signal". While in a general sense, a clock signal might sometimes be considered an "input", in the context of claim 1, an input is recited which is separate from the clock. Therefore the recited "input signal", whatever it is, is something other than the "clock signal". *Bosshart*'s Fig. 4 shows an active device which can

discharge an intermediate node, i.e., feature 26_{DT}, but this device is controlled by the *clock signal*. Therefore, claim1 as amended is not anticipated by *Bosshart*.

Nor is claim 1 obvious over *Bosshart*. *Bosshart* does not even begin to disclose the problem addressed by applicant's invention, or suggest any particular solution. *Bosshart*'s clocked discharge transistor 26_{DT} serves an essential purpose in a dynamic logic circuit, but there is nothing in *Bosshart* that would suggest another discharge transistor controlled by one of the inputs. Such a transistor serves no useful purpose, unless one considers the effect of parasitic bi-polar transistor action in silicon-on-insulator integrated circuits. Such considerations are not taught or suggested by *Bosshart*.

For similar reasons, applicants' claim 17 is neither anticipated by nor obvious over *Bosshart*. Claim 17 recites:

> 1. A method of reducing the effects of parasitic bipolar transistor action in a silicon-on-insulator (SOI) logic circuit during a pre-charge cycle, comprising:
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> coupling an active discharge device to an intermediate node of the SOI logic circuit; and
>
> controlling the conduction of the active discharging device *using a non-clock signal*, whereby the charge at the intermediate node is maintained at a predetermined level during the pre-charge cycle. [emphasis added]

Even if the various recitations concerning SOI logic are ignored, claim 17 plainly recites that the active discharging device is controlled "using a non-clock signal". *Bosshart* shows only a discharge transistor 26_{DT} controlled by the clock signal.

For all of the reasons stated, the independent claims are patentable over the cited art. The remaining claims are dependent and patentable for the same reasons.

In view of the foregoing, applicants submit that the claims are now in condition for allowance and respectfully request reconsideration and allowance of all claims. In addition, the Examiner is encouraged to contact applicant's attorney by telephone if there are outstanding issues left to be resolved to place this case in condition for allowance.

Respectfully submitted,

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